Xilinx Design with VHDL Course Outline

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1. Language History and Versions
2. RTL / Behavioral Coding Styles
3. The HDL Design Process
4. Basic Constructs
    a. Entity
    b. Architecture
    c. Internal Signals
    d. Port Modes
    e. Coding Conventions
5. The VHDL Process
    a. The Combinatorial Process
    b. The Sequential Process
    c. Intro to Data Classes
6. Data Types
    a. Pre-defined Types
    b. The Problem with Type Bit
    c. Standard Logic
    d. The Resolution Function
    e. Vectors
    f. Enumerated Types
    g. Subtypes
7. Arrays
    a. Array Assignments

    b. Aggregates
    c. Concatenation
    d. Records
8. VHDL Operators
    a. Logical Operators
    b. Relational Operators
    c. Relational Operations on Different Size Vectors
9. Sequential Statements
    a. Concurrency
    b. Process Invocation
    c. Process Suspension
    d. Wait Statements
    e. A Detailed Example of the Simulation Cycle
    f. IF, CASE, FOR, WHILE, NEXT, EXIT
    g. Synthesis Issues with Sequential Statements
10. After Clauses
11. VHDL Variables
    a. Use in Algorithms and Loops
    b. The Variable in a Clocked Process
12. Intro to Packages and Subroutines
    a. Package Header and Body
    b. Functions and Procedures
    c. Overloading
13. Arithmetic Packages

14. Data Type Conversion
15. Concurrent Statements
16. Synthesis
    a. Timing Closure
    b. Coding Styles for Synthesis
    c. Synthesis Directives
    d. State Machine Design
17. Simulation
    a. Hierarchy
    b. Compilation Order
    c. Design Units
18. Testbench Design
    a. Standalone Testbenches
    b. DSP Testbenches
    c. Pseudo-code Testbenches
    d. Assertions
19. The Xilinx Architecture
    a. The Logic Cell
    b. Block RAM
    c. DSP Slices
    d. Clocking Resources
    e. I/O Resources
    f. High-Speed Serial I/O
    g. The XADC

    h. Configuration
    i. Xilinx FPGA Families

20. Xilinx Tools
    a. ISE vs. Vivado
    b. ISE Flow
    c. Coregen
    d. Constraint Files

21. Advanced VHDL Features
    a. Attributes
    b. Generics
    c. Generate Statements